Instruction Enhancement Program on Analog & RFIC Design

Under Chip to startup Program
Organised by
Department of Electronics & Communication Engineering
National Institute of Technology Silchar

*Scan the QR Code for redirecting to IEP Registration

The Department of Electronics & Communication Engineering, NIT Silchar, is organizing a 5-day Instruction Enhancement Programme (IEP) on "Analog & RFIC Design" under Chip to Startup Program, supported by the ChipIN Team (CDAC), funded by MeitY, Govt. of India.

Details of IEP

Dates: 24th August 2026 to 28th August 2026
Mode: 5-Day Hybrid-Mode session
Time: Full-Day Sessions
Venue: Department of ECE,NIT Silchar, Assam, India

Topics of IEP

Analog and RFIC Design

HIGHLIGHTS

1. Experts from industry and academia
2. Full tapeout demonstration for analog IC design.
3. RFIC design Challenges
4. Extensive lab sessions
5. Interaction with Industry experts

Acomodation

Hostel/Guest House accommodation will be provided on a payment basis. subject to availability.

Contact Us

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Don't Miss Out! Seats are Limited. Apply Now! to join exciting oppurtunity!
Last Date: on or before 22 August 2026.

Instruction Enhancement Program on Analog & RFIC Design

Tentative Day Wise Schedule

DAY 1	09:00 AM to 11:00AM	Registration and Inauguration
	11:00 AM to 11:15AM	Tea Break
	11:15AM to 1:15PM	Introduction to Analog IC Design and Challenges (Expert Talk)
	1:15PM to 2:00PM	Lunch
	2:00PM to 3:30PM	Design of Folded Cascode Amplifier (FC-Opamp) (Theory)
	3:45PM to 3:45PM	Tea Break
	3:45PM to 5:00PM	Design of FC-Opamp (Hands-on)
DAY 2	09:00 AM to 11:00AM	Energy-Efficient VLSI Architectures and Trends for Biomedical Systems (Expert Talk)
	11:00 AM to 11:15AM	Tea Break
	11:15 AM to 1:15PM	Introduction to Backend Design of Analog blocks and its challenge
	1:15PM to 2:00PM	Lunch
	2:00PM to 3:30PM	Layout & verification session of FC-Opamp (Hands-on)
	3:30PM to 3:45PM	Tea Break
	3:45PM to 5:00PM	Layout & verification session of FC-Opamp (Hands-on)
DAY 3	09:00 AM to 11:00AM	Introduction to RFIC Design and challenges (Expert Talk)
	11:00 AM to 11:15AM	Tea Break
	11:15 AM to 1:15PM	Design and Analysis of Low noise amplifier (LNA) (Theory)
	1:15PM to 2:00PM	Lunch
	2:00PM to 3:30PM	LNA Design (Hands-on)
	3:30PM to 3:45PM	Tea Break
	3:45PM to 5:00PM	LNA Design (Hands-on)
DAY 4	09:00 AM to 11:00AM	Design and discussion of Voltage controlled Oscillators (Theory)
	11:00 AM to 11:15AM	Tea Break
	11:15 AM to 1:15PM	Design and Analysis of Ring VCO (Theory)
	1:15PM to 2:00PM	Lunch
	2:00PM to 3:30PM	Design and Analysis of Ring VCO (Hands-on)
	3:30PM to 3:45PM	Tea Break
	3:45PM to 5:00PM	Design and Analysis of Ring VCO (Hands-on)
DAY 5	09:00 AM to 11:00AM	Design and Analysis of Pre-Scalar (Theory)
	11:00 AM to 11:15AM	Tea Break
	11:15 AM to 1:15PM	Design and Analysis of Pre-Scalar (Theory)
	1:15PM to 2:00PM	Lunch
	2:00PM to 3:30PM	Design and Analysis of Pre-Scalar (Hands-on)
	3:45PM to 5:00PM	Doubt Clearance & Valedictory Function

Online session link will be provide after registration

Instructions for Participants

- **It is mandatory for one faculty (CI/Co-CI) from each C2S organization to attend the IEP.**
- **If seats are available, additional faculty (CI/Co-CI) from the same C2S institute can be accommodated.**
- **All materials related to the reference design for the IEP sessions will be provided to the C2S participants.**
- **Accommodation, travel to/fro from their city to the venue, as well as local travel to/fro airport/station to lodging, should be managed by participants from respective Institute's C2S project heads.**
- **Participants need to bring their own laptops (Preferable). Minimum Requirement of 8 GB RAM and 256 GB Hard Disk Free Space. (OS: Windows 10 or above).**